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PATTERN AND POSITION DEPENDENT GATE LEAKAGE AND REDUCTION TECHNIQUE

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Abstract

The leakage power has become a vital downside in modern VLSI technology, with the advent in the area of high performance chips and portable electronics. Thus it is necessarily to invest more time and effort in designing low power chip without sacrificing its high performance. This paper describes a steady state gate leakage based on position and biasing states. As a basic reference universal gates are selected and compared the gate leakage of conventional NAND and NOR gate using 180nm TSMC technology. It is shown that the overall leakage in a NAND -gate is smaller than in a NOR gate if equal size transistors are used. It also compares the leakage value of proposed leakage reduction techniques with conventional NAND gate. Simulation results shows up to 88% in average gate leakage reduction with modified techniques.

Keywords:

Leakage Power, Gate Leakage, QMDT, Direct Tunneling

1. INTRODUCTION

The rate of increase in the memory requirement as well as the rate of increase in the total amount of memory per chip has more than kept pace with the rate of reduction in power dissipation per bit of memory. Now a day, with the growing trend towards portable wireless and computing communication, power dissipation has become one of the most critical factors in the submicron technology. At different levels of design abstractions it is important to estimate both maximum and average power in CMOS circuits. The maximum power and the average power is playing an important role to determine reliability and battery life respectively. As technology scales down the threshold voltage (V_{th}) must be reduced at the same rate to restrain power density and gate overdrive [1]. As the supply voltage is reduced while the threshold voltages stay the same reduced noise margin (NM) result. To improve NM the threshold voltages need to be made smaller.The lower the threshold voltage the lower the degree to which MOSFETs in the logic gates are turned off and the higher is the leakage current. Consequently, the modelling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. The higher static dissipation may offset the reduction in transitions component of the dissipation. Hence the devices need to be designed to have threshold voltages that maximize the net reduction in the dissipation. In short channel devices, the off-state current is influenced by threshold voltage, channel physical dimensions, surface doping profile,drain and source junction depths, gate oxide thickness, gate voltage and supply voltage.

Reducing the transistor's gate length when no voltage is applied at gate results in more leakage current between source and drain of the transistor which eventually results in the more power consumption [2]. In past technologies the leakage current is usually neglected as the magnitude of leakage current was low. As a consequence of device scaling leakage current in the nanometre regime is becoming significant portion of power dissipation in CMOS circuits, as depicted in Fig.1.

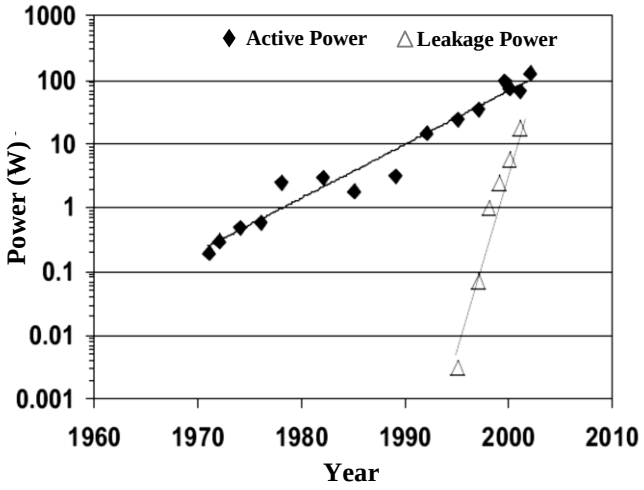

Fig.1. Dynamic and Static power dissipation [3]

The various sources for the leakage current are [4] such as the gate leakage current due to very thin gate oxide and sub-threshold leakage current due to low V_{th}. The sub-threshold leakage current is the drain-to source leakage current when the transistor is in the OFF mode. This leakage is important, when the gate to source voltage of a transistor is less than the threshold voltage of the transistor. As V_{th} is scaled down with technology scaling, gate leakage increases exponentially with decreasing oxide thickness. This leakage flows from the gate terminal through the oxide to the substrate. Gate leakage current of transistor increases exponentially with the reduction of the T_{ox} over the active region of the transistor [5]. Gate oxide leakage, occurs in both cases, when transistors are turned on and off. This current is independently for both, turned on or off, transistor states. On the other hand sub-threshold leakage is occurs only when transistor is turned off.

Many leakage reduction techniques are present to reduce leakage power in the circuit at significant level. This paper describes a circuit level leakage reduction approaches [6] to reduce runtime leakage by modifying logic gates, designed in nano-scale regime. Here NAND gate is selected as a basic reference. The oxide thickness scales below 1.8nm [7], a significant fraction of the conventional off-state leakage current will be due to gate

leakage near the drain portion of the devices. When the gate becomes thinner large tunnelling hinders the formation of the inversion layer and the drain current does not increase. Gate leakage is predicted to increase at a rate of more than 500X per technology generation, while sub-threshold leakage increases by around 5X for each technology generation [8].

The organization of the paper is as follows: The section 2, describes the different components of gate leakage. Section 3 presents structure dependent gate leakage estimation. The simulation study of conventional NAND has mentioned in section 4. A comparative study of NAND and NOR has been made in section 5. In section 6 the detail of the proposed technique and its result are discussed. Finally the conclusion is presented in section 7.

2. GATE OXIDE TUNNELING MODEL

The continuous down scaling of the device size lead to reduce the gate oxide thickness to nano meters causes a flow of leakage current between substrate and the gate through the oxide. Thus the gate tunneling current comes in to the order of the sub threshold leakage current. In the nanoscale MOSFETs, the oxide thickness is the order of a few angstroms and further scaling down is not possible with the existing technology. This increases the standby power consumption due to the static gate current. Two tunneling are responsible for the gate leakage-FN tunneling (Fowler-Nordheim) and direct tunneling. For lower value of gate voltage, F-N tunneling occurs owing to the conduction of electron from the conduction band of Si substrate to the conduction band of the poly-si gate through the triangular conduction band of the SiO_2. F-N current density is very important parameter in the non-volatile memory applications. The F-N current density is given by,

$$J_{FN} = C_{FN} E_{ox}^2 \exp^{-\left(\frac{B}{E_{ox}}\right)} \quad (1)$$

where, $\beta = 8\pi(2m_{0x})^{\frac{1}{2}} \varphi_b^{\frac{3}{2}} \Big/ 3qh$, $C_{FN} = \frac{q^2 m_o}{8\pi h m_{ox} \varphi_b}\left(\frac{A}{V^2}\right)$ and E_{ox} is the electrical field in the oxide.

The electric field existing at the ultrathin gate oxide (4nm or less) is so high that tunneling takes place directly through the energy barrier of the diode. This quantum mechanical direct tunneling in the gate oxide (QMDT) is more complicated as compared with the F-N tunneling. Indirect tunneling oxide conduction band potential is trapezoidal in nature. The Fig.2 explains the direct tunneling phenomenon between a polysilicon gate and a p-substrate.

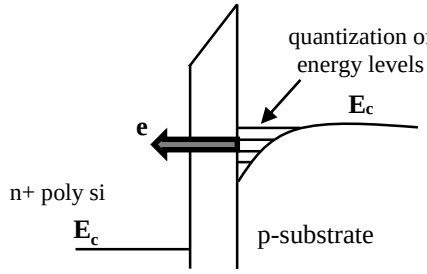

Fig.2. Direct tunneling of electrons

In the thin oxide regime, the QMDT will be exponentially increased as in Eq.(2) leading to significant power dissipation and performance deterioration,

$$J_{DT} = A\left(\frac{V_{ox}}{T_{ox}}\right)^2 \exp\left[\frac{-B\left(1-\left(1-\frac{V_{ox}}{\phi_{ox}}\right)\right)^{\frac{3}{2}}}{\frac{V_{ox}}{T_{ox}}}\right] \quad (2)$$

where, A and B are physical parameters given by Eq.(3)

$$A = \frac{q^3}{16\pi^2 \hbar \phi_{ox}} \text{ and } B = \frac{4\sqrt{2m^*}\,\phi_{ox}^{\frac{3}{2}}}{3\hbar q} \quad (3)$$

where, J_{DT} is the direct tunneling current density, V_{ox} is the potential drop across the thin oxide, ϕ_{ox} is the barrier height for the tunneling particle and T_{ox} is the oxide thickness, m^* is the effective mass of the tunneling particle, q is the electron charge and $\hbar$ is the planck constant.

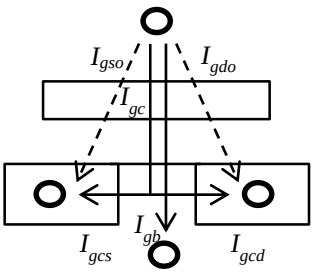

Fig.3. Tunneling current component

The net oxide current is the summation of the F-N tunneling current and direct tunneling current. The F-N is very small and can be neglected. The Fig.3 shows the various current components of gate tunneling in a nano scale MOSFETs. This current is composed of several components. The gate tunneling current (I_g) can be divided into three major components;

1. Gate-to-Drain ($I_{gd} = I_{gdo} + I_{gcd}$)
2. Gate-to-Substrate (I_{gb})
3. Gate-to-Source ($I_{gs} = I_{gso} + I_{gcs}$)

where, I_{gc} is the gate-to-inverted channel tunneling current. Part of I_{gc} is collected by the source (I_{gs}) while rest goes to the drain (I_{gd}). I_{gso} and I_{gdo} are parasitic leakage currents through gate to source/drain extension overlap region and I_{gb} is the gate-to-substrate leakage current. In contrast to sub threshold currents, gate tunneling currents are present in both on and off stages of the transistor. This oxide leakage results in low drain currents and hence the operation of the circuit at low power is seriously hampered.

3. STRUCTURE DEPENDENT GATE LEAKAGE

Circuit topology is a primary determined of the overall leakage current. In [9] authors describe techniques to reduce leakage current in the deep submicron CMOS circuits. The gate leakage is an exponential function of the gate oxide field. Thus the gate current shows an exponential dependence on the gate to

source (V_{GS}) bias. The position of a specific transistor in relation to other transistors in a given structure determines whether it operates in strong inversion or at the threshold when switched on.In the following analysis, steady-state gate leakage estimation based on state characterization [10] is used to find the spice level gate leakage current for universal gates. Based on that a gate leakage reduction circuit technique was proposed. This work considers four possible biasing states, out of eight biasing states to find the gate leakage. The possible bias conditions for an NMOS transistor at steady state are shown in Fig.4. The two stages out of four, namely <101> and <110> at the gate, drain and source of the transistor are transient states, as these stages cannot occur in steady states. The remaining two stages, namely <000> and <111> are considers as a non-leaky stages. Given an input vector, it is possible to perform a switch level simulation to determine the state of the internal nodes of the circuits. Here it is assumed that the internal nodes attain full logic level (i.e. either V_{DD} or V_{SS}). Here both forward and backward gate leakage PMOS and NMOS transistors are considered.

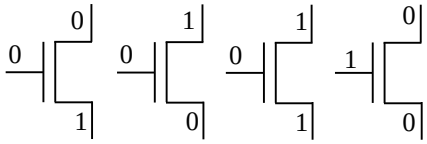

Fig.4. Four leaky bias conditions for a NMOS transistor

4. NORMAL CMOS NAND GATE

NAND is a universal gate using which all other gates can be constructed. Its output is low whenever both inputs (A and B) are high. In Fig.5 NMOS are connected in series between V_{DD} supply and output $V_{OUT,}$ while the PMOS are connected parallel between V_{DD} supply and output V_{OUT}.

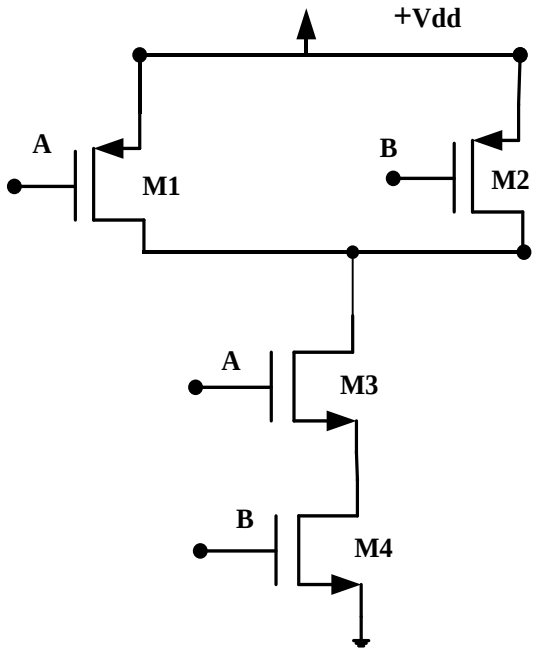

Fig.5. CMOS NAND gate

The structure dependent leakage current of NAND gate using BSIM spice simulation (180nm TSMC) is tabulated in Table.1.

Table.1. NAND gate leakage current

	NAND1 $L_n = L_p = 0.2\mu$	**NAND2** $L_n = L_p = 0.2\mu$	
Width (μm)	$W_n = 1$, $W_p = 2$	$W_n = 2$, $W_p = 6$	
Input	**$I_{leak1(\eta A)}$**	**$I_{leak2(\eta A)}$**	**% increase**
00	0.02	1.2	98
01	6.626	48.7	86.3
10	0.984	2.5	60.6
11	17.9	81.4	78
Average Leakage (nA)	6.38	33.3	80.8

When a device in a NMOS transistor stack is off, there exists no conducting path from V_{DD} to the drain terminal of the device below it and hence these nodes can be assumed to be nearly at ground potential. The gate of the leaky device acts like a resistor connected between V_{DD} and V_{SS} lines. The total leakage of the circuit is the sum of the gate leakage of the individual devices. The Fig.6 shows maximum leakage for input combination A = B = 1, and minimum for A = B = 0.

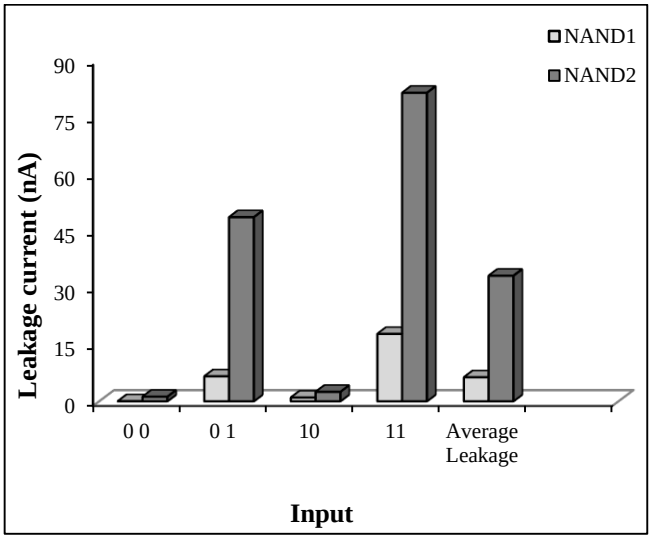

Fig.6. NAND gate leakage current

5. COMPARING NOR AND NAND STRUCTURES

In a NOR gate, NMOS transistors are connected in parallel is used as pull up circuit and PMOS transistors are connected in series is used as pull-down circuit shown in Fig.7.

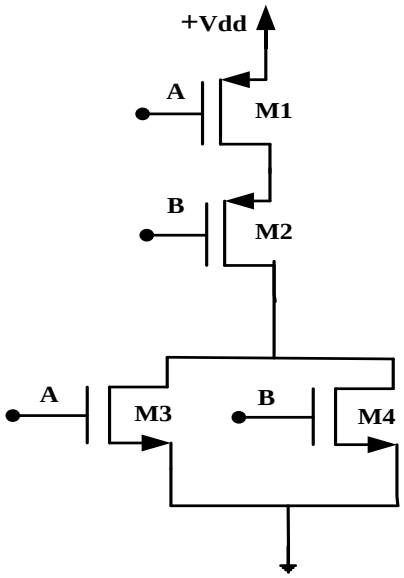

Fig.7. CMOS NOR gate

Here, each transistor leaks when turned on, independently from others. In leakage sense, this structure is a 'worst case' structure.

Table.2. NAND and NOR Gate Leakage

	NAND $L_n = L_p = 0.2\mu$	**NOR** $L_n = L_p = 0.2\mu$
Width (μm)	$W_n = 1$, $W_p = 2$	$W_n = 2$, $W_p = 6$
Input	$\mathbf{I_{leak(\eta A)}}$	$\mathbf{I_{leak(\eta A)}}$
00	0.02	21.6
01	6.626	1.6
10	0.984	18.3
11	17.9	34.7
Average Leakage	6.38	19.03

The leakage current in the NOR and NAND structures for different input combinations are given in Table.2. As in Fig.8 it is shown that gate leakage of NAND structure (stacked NMOS) is less than that of a NOR structure in one out of 3 possible states, corresponding to the inputs (A, B) = (0, 0), (1, 0), (1, 1). PMOS transistors leakage is much less than NMOS transistors, it follows that the overall leakage in a NOR gate is larger than in NAND gate, if equal size transistors are used. The main tunneling component in a PMOS transistor is holes, tunneling from the valence band whichresults in PMOS gate current being roughly 10 times smaller than NMOS current.

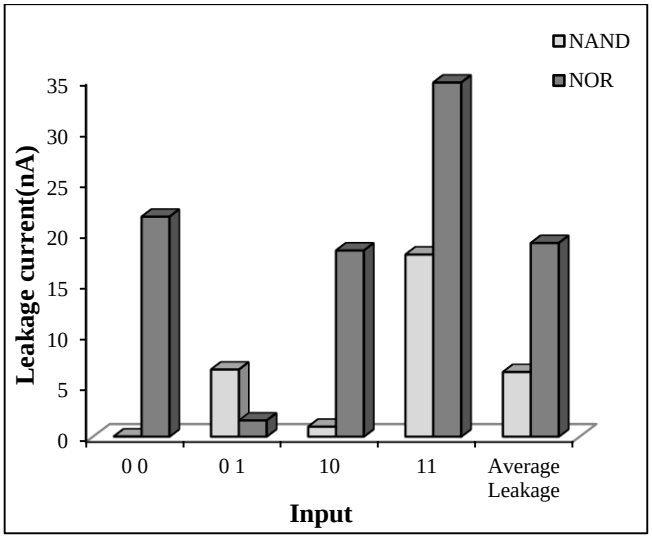

Fig.8. NAND and NOR gate Leakage current

6. MODIFIED CMOS NAND GATE

A gate leakage reduction technique [11], [12] is shown below. Three new components are added in this modified CMOS NAND structure shown in Fig.9. Two NMOS transistors are connected in series with the pull down circuit and one capacitor in the series path from V_{DD} to ground. The minimal leakage is sufficient enough to charge the capacitor to V_{DD} with a time constant set by the circuit parameters. Series combination of two NMOS transistors has been placed with the capacitor.

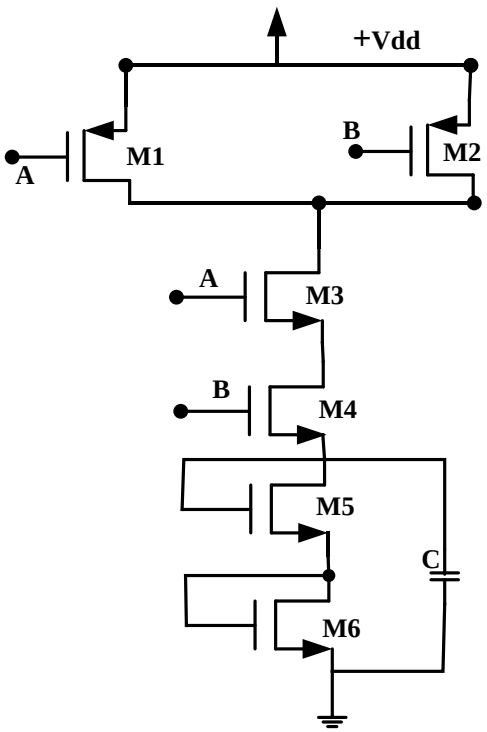

Fig.9. Modified NAND gate

When both inputs are high, the extra two transistors are driven in to saturation, providing a low resistance path for the capacitor

to discharge. Thus the overall functionality of the circuit is unaffected. The value of the capacitor is selected as 1pf.

Table.3. Gate leakage of normal and modified NAND gate

	Normal NAND $L_n = L_p = 0.2\mu$	**Modified NAND** $L_n = L_p = 0.2\mu$	
Width(μm)	$W_n = 2$, $W_p = 6$	$W_n = 1$, $W_p = 3$	
Input	**Leakage Current (ηA)**	**Leakage Current (ηA)**	**% decrease**
00	1.2	0.05	95.8
01	48.761	5.16	89.4
10	2.5	2	20
11	81.37	8.9	89
Average	33.33	4	88

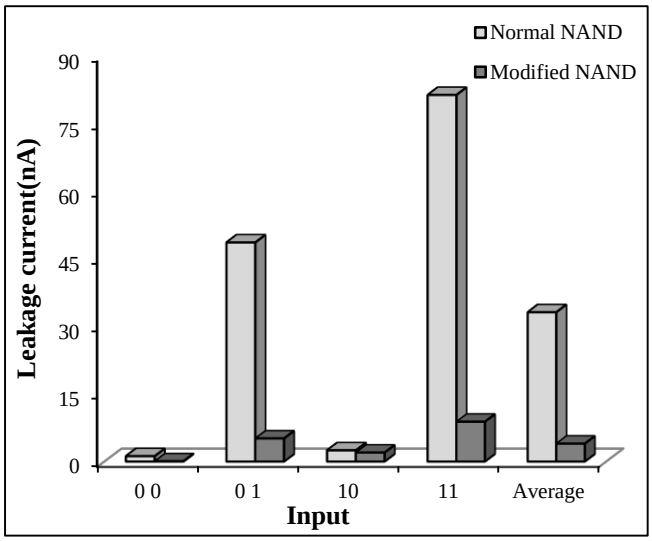

Fig.10. Leakage reduction of proposed one

The experimental result obtained is tabulated in Table.3 and Fig.10. All pre layout simulation has been performed with BSIM using 180nm TSMC technology file. The result shows that the proposed one gives better leakage reduction compared to the normal one. From Table.3 it is observed that the average leakage reduction of 88% is obtained with modified circuit.

7. CONCLUSION

The comparison of leakage current measurement of NAND and NOR gate has been done. It shows that overall leakage in a NOR gate is larger than in a NAND gate. It also shows that transistor sizing is plays an important role for leakage reduction. Modified circuit for NAND gate is proposed to target the lower leakage current. This configuration exhibits larger leakage reduction. Average leakage reduction of 88% is obtained with modified circuit.

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